TEST REPORT

Testing for the verification of compliance of GRID connected POWER CONVERSION SYSTEM with:

Short Duration Undervoltage response test：28 July 2020

Report Reference No…… ...:	200902099GZU-004
Date of issue ……:	17 Sep 2020
Total number of pages……:	35 pages

Testing Laboratory	Intertek Testing Services Shenzhen Ltd. Guangzhou Branch
Address.....	Room 02, & 101/E201/E301/E401/E501/E601/E701/E801 of Room 01 1-8/F., No. 7-2. Caipin Road, Science City, GETDD, Guangzhou, Guangdong, China
Testing location/ address.....	Same as above
Tested by (name + signature)……:	Sunny Lin Engineer
Approved by (+ signature).....	Jason Fu Technical Team Leader

Applicant's name	Shenzhen SOFAR SOLAR Co., Ltd.
Address.....	401, Building 4, AnTongDa Industrial Park, District 68, XingDong Community, XinAn Street, BaoAn District, Shenzhen, China

Test specification:	
Standard	Short Duration Undervoltage response test：28 July 2020
Test procedure.....	Type approval
Non-standard test method……..:	N/A

Test Report Form No.	VDRT_a
Test Report Form(s) Originator	Intertek Guangzhou
Master TRF	Dated 2020-09

Test item description	Solar Grid-tied Inverter
Trade Mark.....	SOFAR SOLAR
Manufacturer.....	Same as Applicant
Model/Type reference.....	SOFAR 10000TL-G2, SOFAR 12000TL-G2, SOFAR 15000TL-G2

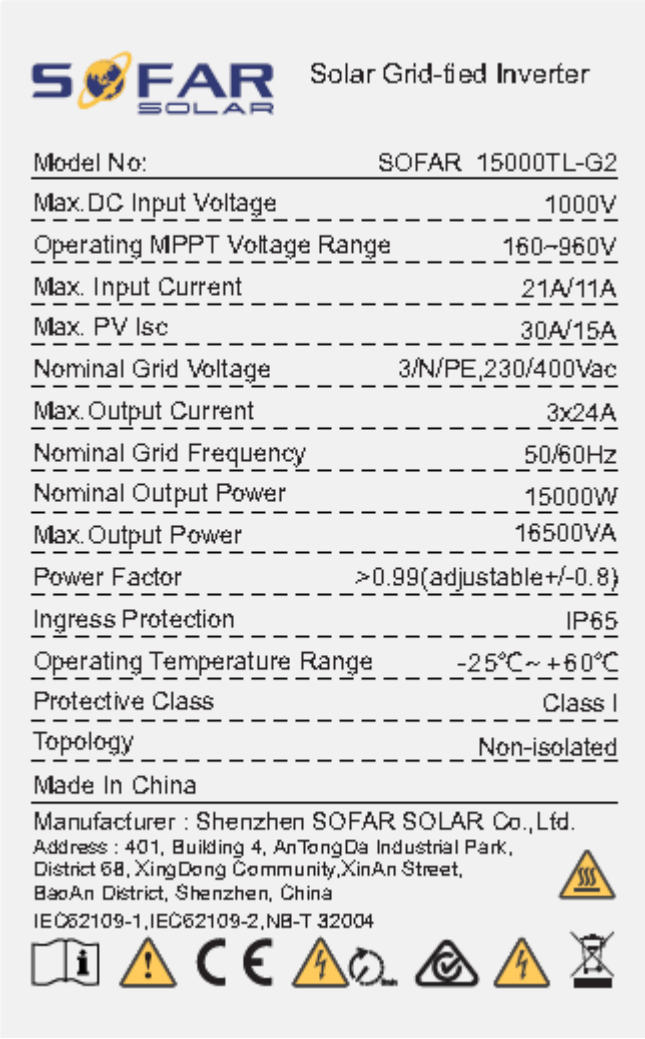
Ratings .....

Model	SOFAR 10000TL-G2	SOFAR 12000TL-G2	SOFAR 15000TL-G2
Max.PV voltage	1000 d.c.V		
PV MPPT voltage range	160-960 d.c.V		
Max.input current	21 /11 d.c.A		
PV Isc	30/15 d.c.A		
Max.output power	10000W	12000W	15000W
Max.apparent power	11000VA	13200VA	16500VA
Nominal output voltage	3/N/PE, 230 /400 a.cV		
Max.output current	3×16.5 a.c.A	3×20.0 a.c.A	3×24.0 a.c.A
Nominal output Frequency	50 Hz		
Power factor range	0.8Leading – 0.8 lagging		
Inverter technology	Non-isolated		
Safety level	Class I		
Ingress Protection	IP 65		
Operation Ambient Temperature	-25℃ - +60℃		
Software Version	V0.21		

Summary of testing:

Tests performed (name of test and test clause):	**Testing location:**
All applicable tests The model SOFAR 15000TL-G2 is type tested. For certification testing for compliance with AS/NZS 4777.2:2015 refer to report No. 190411091GZU-003, dated 18 Jun 2019, issued by Intertek Testing Services Shenzhen Ltd. Guangzhou Branch.	Intertek Testing Services Shenzhen Ltd. Guangzhou Branch Room 02, & 101/E201/E301/E401/E501/E601/E701/E801 of Room 01 1-8/F., No. 7-2. Caipin Road, Science City, GETDD, Guangzhou, Guangdong, China

Copy of marking plate



Note:

1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
2. Label is attached on the side surface of enclosure and visible after installation
3. The other model labels are identical with label above, except the model name and rating.

Test item particulars.....:	
Temperature range .....:	-25℃ - 60℃
AC Overvoltage category.....:	☐ OVC I ☐ OVC II ☒ OVC III ☐ OVC IV
DC Overvoltage category .....:	☐ OVC I ☒ OVC II ☐ OVC III ☐ OVC IV
IP protection class .....:	IP 65
Possible test case verdicts:	
- test case does not apply to the test object..... :	N/A (Not applicable)
- test object does meet the requirement ..... :	P (Pass)
- test object does not meet the requirement ..... :	F (Fail)
Testing..... :	
Date of receipt of test item..... :	04 Sep 2020
Date (s) of performance of tests..... :	04 Sep 2020 – 08 Sep 2020

General remarks:

The test results presented in this report relate only to the object tested.
This report shall not be reproduced, except in full, without the written approval of the Issuing testing laboratory.
"(see Enclosure #)" refers to additional information appended to the report.
"(see appended table)" refers to a table appended to the report.

When determining for test conclusion, measurement uncertainty of tests has been considered.
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The test report only allows to be revised only within the report defined retention period unless standard or regulation was withdrawn or invalid.

Throughout this report a point is used as the decimal separator.

General product information:

The unit is a three-phases non-isolated PV Grid-tied inverter, it can convert the high PV voltage to Grid voltage and feed into Grid network.

The unit is providing EMI filtering at the PV side and AC side. It does provide basic insulation from PV side to Grid.

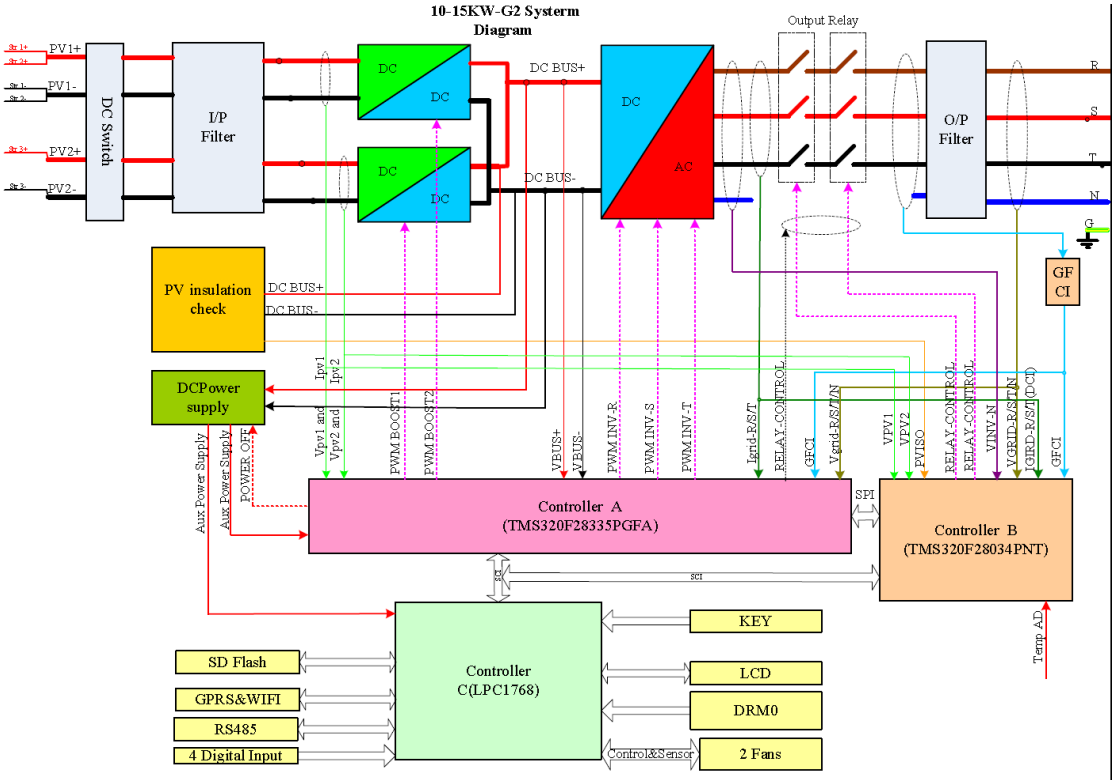
The unit has two controllers. The master controller A monitor the invert statue; measure the PV voltage and current, bus voltage, AC voltage, current, GFCI and frequency, also communicate with the slave controller B

The slave controller B monitor AC voltage, current, frequency, GFCI and communicate with the master controller A

The relays are designed to redundant structure that controlled by separately.

The master controller and slave controller are used together to control relay open or close, if the single fault on one controller, the other controller can be capable to open the relay, so that still providing safety means.

The topology diagram as following:



Model differences:

The model SOFAR 10000TL-G2, SOFAR 12000TL-G2 and SOFAR 15000TL-G2 are completely identical, except output power derating in software.

The only differences on hardware between the models SOFAR 10000TL-G2, SOFAR 12000TL-G2 and SOFAR 15000TL-G2 are below:

1.The main output inductor is NPS226060*2+NPF226060*2, 2.0Φ*2P /37Ts L=756μH for model SOFAR 15000TL-G2 while it's NPS226060*2+NPF226060*1, 2.0Φ*2P*42Ts L=0.73mH for model SOFAR 10000TL-G2, SOFAR 12000TL-G2

Other than special notes, typical model SOFAR 15000TL-G2 is used as representative for testing in this report

Version of software: V0.21

Version of hardware: V1.00

Short Duration Undervoltage response test			
Clause	Requirement – Test	Result – Remark	Verdict
1	General test and reporting requirements		P
1.1	General		P
1.2	Test condition		P
1.3	Inverter setup		P
1.4	Grid source		P
2	Test procedure		P
2.1	General		P
2.2	Undervoltage(V<) disconnection test in response to event duration exceeding trip delay time		P
2.3	Undervoltage(V<) withstand test in response to event duration of less than trip delay time		P
2.4	Criterial for acceptance		P

1.1 Customer Equipment

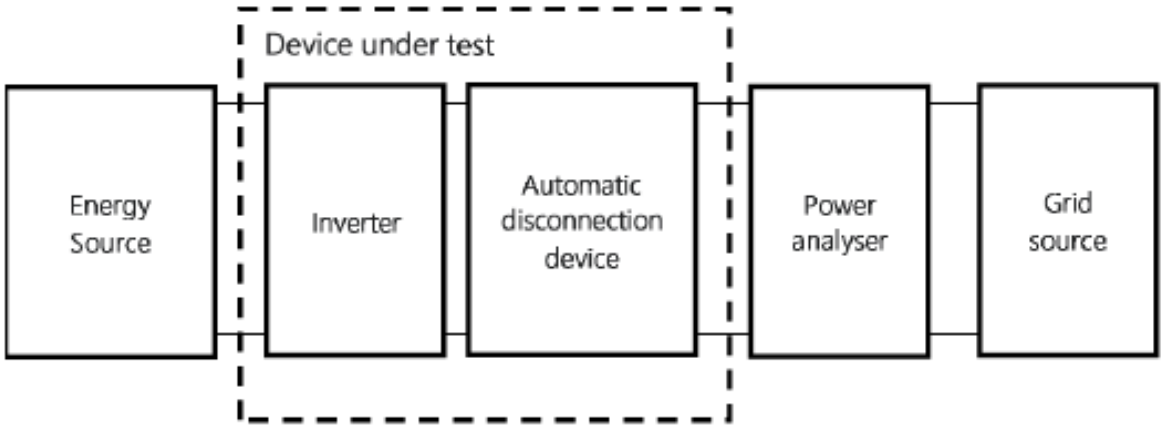
Equipment	Manufacturer	Type	Serial No.
PV Inverter	Shenzhen SOFAR SOLAR Co., Ltd.	SOFAR 15000TL-G2	SN1CS015K1R081

1.2 Intertek Equipment

Asset	Description	Manufacturer	Model	Cal Date	Cal Due
SA200-16	Precision Power Analyzer	YOKOGAWA	WT3000	12 Aug 2019	11 Aug 2020
SA200-52	AC power source	Chroma	61860	/	/
SA050-33	Scope recorder	YOKOGAWA	DL 850E	31 Oct 2019	30 Oct 2020
SA050-33-01	AC Current Probe	Chauvin Arnoux	C173	14 Jan 2020	13 Jan 2021
SA050-33-02	AC Current Probe	Chauvin Arnoux	C173	14 Jan 2020	13 Jan 2021
SA050-33-03	AC Current Probe	Chauvin Arnoux	C173	14 Jan 2020	13 Jan 2021
SA200-18	TopCon series DC power supply	REGATRON	TC.P.32.1000.400.PV.HMI	07 Aug 2020	06 Aug 2021

2. Test set up & Test Conditions

Below is the simplified construction of the test set up used in all tests of this report.



Test Conditions		
Condition	**Value**	**Comments**
the average r.m.s. current on each phase is within ±5 % of the intended test point;	50% ±5 %In	--
the average r.m.s. voltage on each phase is within ±1 % of the grid test voltage	See test result	--
For three-phase supply, the angle between the fundamental voltages of each pair of phases shall be maintained at 120 ± 1.5°.	Complies	Three-phase
For three-phase supply, the average r.m.s. voltages between each pair of phases shall be maintained within ±1 %.	Complies	Three-phase
The grid test voltage shall be 230 V a.c. phase to neutral, 50 ± 0.1 Hz	230V,50Hz	--
AC source used for test	See equipment list	simulated test grid
The impedance of the test point should not cause a voltage rise greater than 0.5 % of the grid test voltage at the rated current output of the device under test.	Voltage at no load condition: 230.08V/230.13V/230.011V Voltage at full load condition: 230.33V/230.63V/230.58V	--
Note 1: These test conditions have been used in all the test performed in Sections 3.1 to 3.2 of this report.		

2.1. Voltage harmonic for Test bench

The real grid or a simulated test grid should be free from harmonic distortion which could interfere with testing. The voltage harmonic distortions of the real or simulated test grid shall be less than the limits specified in the table below.

Harmonic order number	Limit based on percentage of fundamental
3	0.9 %
5	0.4 %
7	0.3 %
9	0.2 %
Even harmonics 2–10	0.2 %
11–50	0.1 %
Total harmonic distortion (to the 50th harmonic)	5 %

Nr./ Order	Phase A U_h(%)	Phase B U_h(%)	Phase C U_h(%)	Limited (%)
2	0.0080	0.0220	0.0110	0.2
3	0.0150	0.0170	0.0150	0.9
4	0.0030	0.0010	0.0010	0.2
5	0.0190	0.0200	0.0190	0.4
6	0.0020	0.0030	0.0020	0.2
7	0.0090	0.0120	0.0080	0.3
8	0.0020	0.0010	0.0020	0.2
9	0.0060	0.0050	0.0040	0.2
10	0.0030	0.0010	0.0050	0.2
11	0.0010	0.0010	0.0030	0.1
12	0.0020	0.0020	0.0020	0.1
13	0.0010	0.0030	0.0010	0.1
14	0.0020	0.0050	0.0010	0.1
15	0.0030	0.0030	0.0040	0.1
16	0.0030	0.0010	0.0040	0.1
17	0.0000	0.0010	0.0020	0.1
18	0.0030	0.0010	0.0030	0.1
19	0.0010	0.0020	0.0010	0.1
20	0.0010	0.0010	0.0020	0.1
21	0.0020	0.0030	0.0030	0.1
22	0.0020	0.0020	0.0030	0.1
23	0.0030	0.0030	0.0030	0.1
24	0.0020	0.0010	0.0010	0.1
25	0.0020	0.0020	0.0010	0.1
26	0.0010	0.0010	0.0020	0.1
27	0.0030	0.0030	0.0040	0.1
28	0.0020	0.0020	0.0020	0.1
29	0.0030	0.0010	0.0040	0.1
30	0.0020	0.0020	0.0020	0.1
31	0.0020	0.0020	0.0020	0.1
32	0.0040	0.0020	0.0030	0.1

33	0.0030	0.0020	0.0010	0.1
34	0.0020	0.0010	0.0010	0.1
35	0.0030	0.0020	0.0030	0.1
36	0.0010	0.0010	0.0010	0.1
37	0.0030	0.0020	0.0030	0.1
38	0.0030	0.0020	0.0020	0.1
39	0.0030	0.0010	0.0000	0.1
40	0.0050	0.0010	0.0020	0.1
41	0.0030	0.0030	0.0010	0.1
42	0.0010	0.0030	0.0020	0.1
43	0.0020	0.0010	0.0040	0.1
44	0.0020	0.0020	0.0020	0.1
45	0.0000	0.0010	0.0020	0.1
46	0.0130	0.0050	0.0040	0.1
47	0.0010	0.0010	0.0020	0.1
48	0.0100	0.0070	0.0050	0.1
49	0.0020	0.0000	0.0020	0.1
50	0.0020	0.0010	0.0020	0.1
THD (%)	0.052	0.059	0.054	5

3. Test result

3.1 Undervoltage(V<) disconnection test in response to event duration exceeding trip delay time

Grid source voltage	230.0V	Test at 50 ±5% rated output current (A):	11.18/11.28/11.38

All three phases

Test step	Grid source voltage Setting (V)	Grid source voltage measured (V)			Disconnection time (s) (*) 1s<t<2s			Reconnection time (s) t >60s		
		Test 1	Test 2	Test 3	Test 1	Test 2	Test 3	Test 1	Test 2	Test 3
a)	177.5	177.21/ 177.51/ 177.25	176.92/ 176.92/ 176.92	176.58/ 176.46/ 176.50	1.225	1.230	1.230	--	--	--
b)	230	230.13/ 230.33/ 230.04	230.18/ 230.08/ 230.21	230.10/ 230.25/ 229.96	--	--	--	83.49	83.34	81.23

Phase L1

Test step	Grid source voltage Setting (V)	Grid source voltage measured (V)			Disconnection time (s) (*) 1s<t<2s			Reconnection time (s) t >60s		
		Test 1	Test 2	Test 3	Test 1	Test 2	Test 3	Test 1	Test 2	Test 3
a)	177.5	177.54	177.58	177.55	1.235	1.220	1.200	--	--	--
b)	230	230.14	230.12	230.21	--	--	--	82.47	82.90	82.82

Phase L2

Test step	Grid source voltage Setting (V)	Grid source voltage measured (V)			Disconnection time (s) (*) 1s<t<2s			Reconnection time (s) t >60s		
		Test 1	Test 2	Test 3	Test 1	Test 2	Test 3	Test 1	Test 2	Test 3
a)	177.5	177.58	177.59	177.52	1.230	1.220	1.240	--	--	--
b)	230	229.98	230.16	230.01	--	--	--	83.50	84.90	85.45

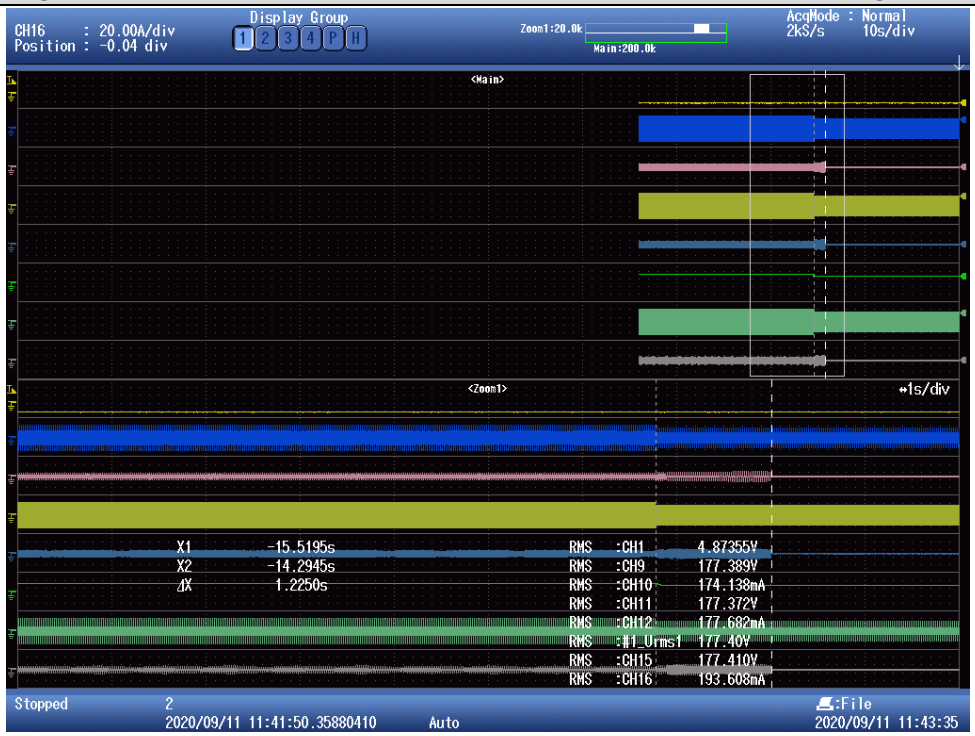
Phase L3

Test step	Grid source voltage Setting (V)	Grid source voltage measured (V)			Disconnection time (s) (*) 1s<t<2s			Reconnection time (s) t >60s		
		Test 1	Test 2	Test 3	Test 1	Test 2	Test 3	Test 1	Test 2	Test 3
a)	177.5	177.55	177.53	177.58	1.200	1.260	1.200	--	--	--
b)	230	230.12	230.20	230.15	--	--	--	84.20	84.85	84.20

Note:
(*) The disconnection time recorded shall be greater than the trip delay time of AS4777.2:2015 of 1 s and less than the disconnection time of AS4777.2:2015 of 2 s

	Voltage drop time measured	Voltage drop time Limited
230V→177.5	1.0ms	2ms

Undervoltage (V<) disconnection test in response to event duration exceeding trip delay time

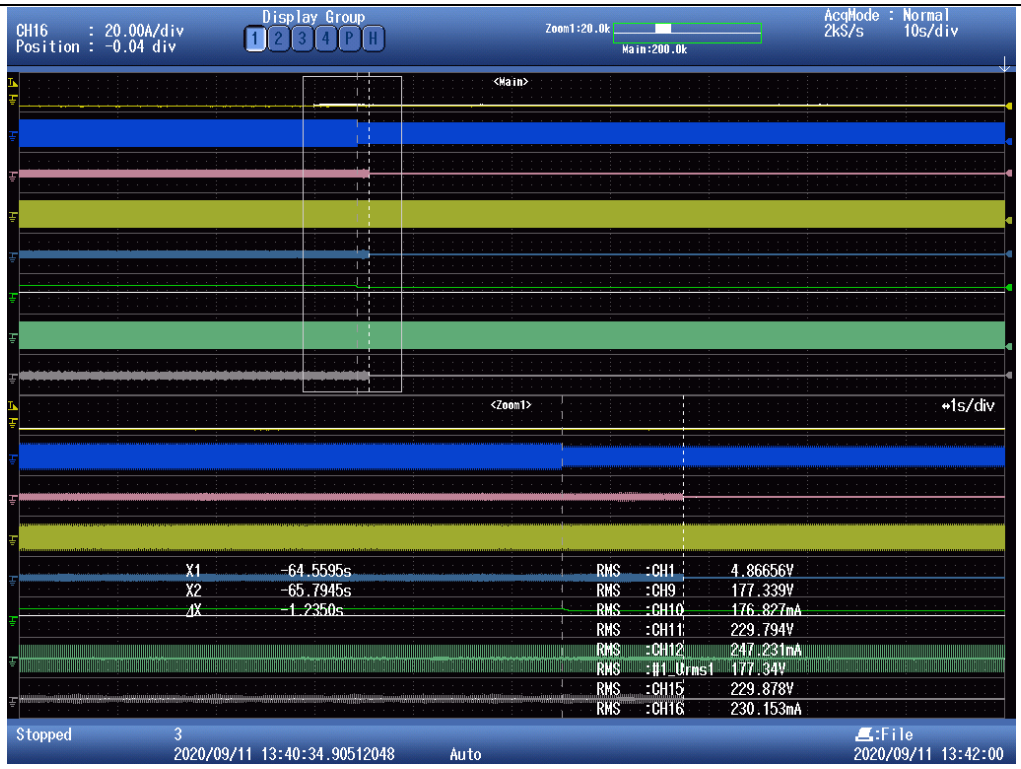


Test 1: All phases disconnection time

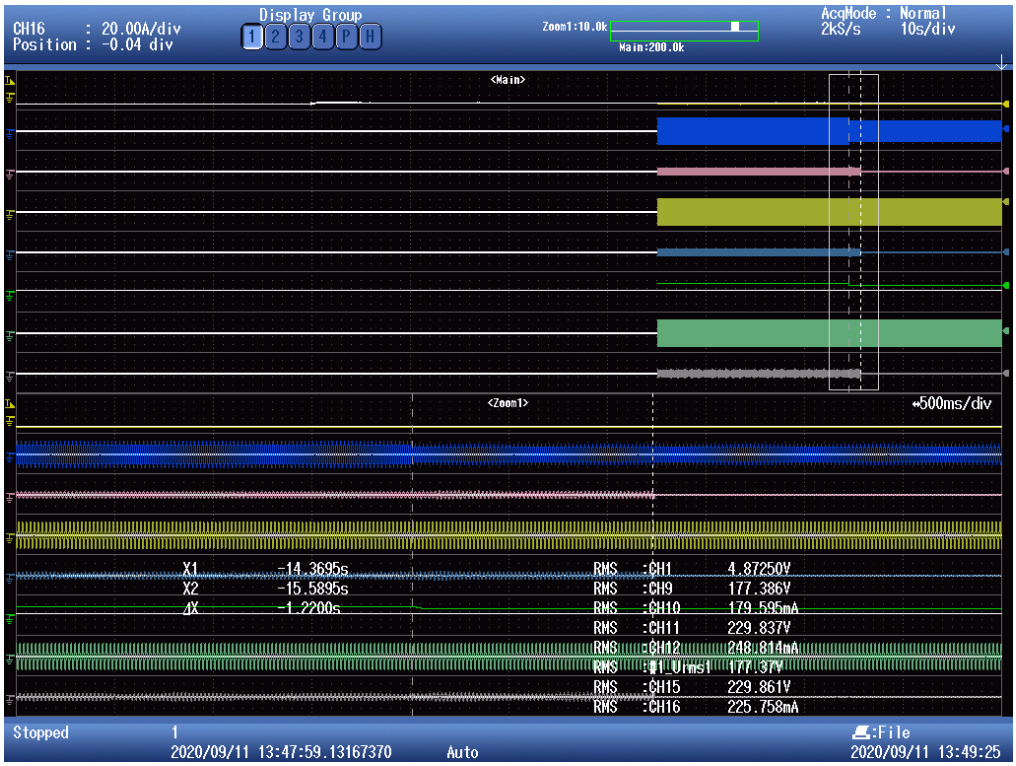
CH1: trip signal; CH9, CH11, CH15: Grid Voltage; CH10, CH12, CH16: Current of EUT

Test 2: All phases disconnection time

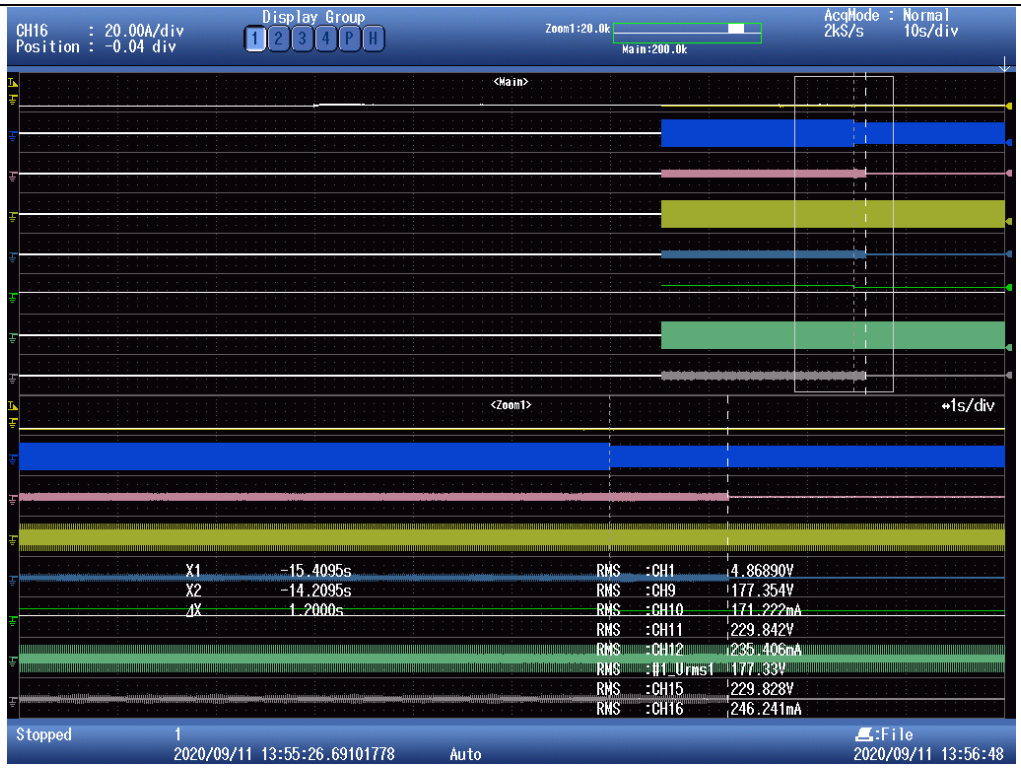
Test 3: All phases disconnection time



Test 1: Phases L1 disconnection time



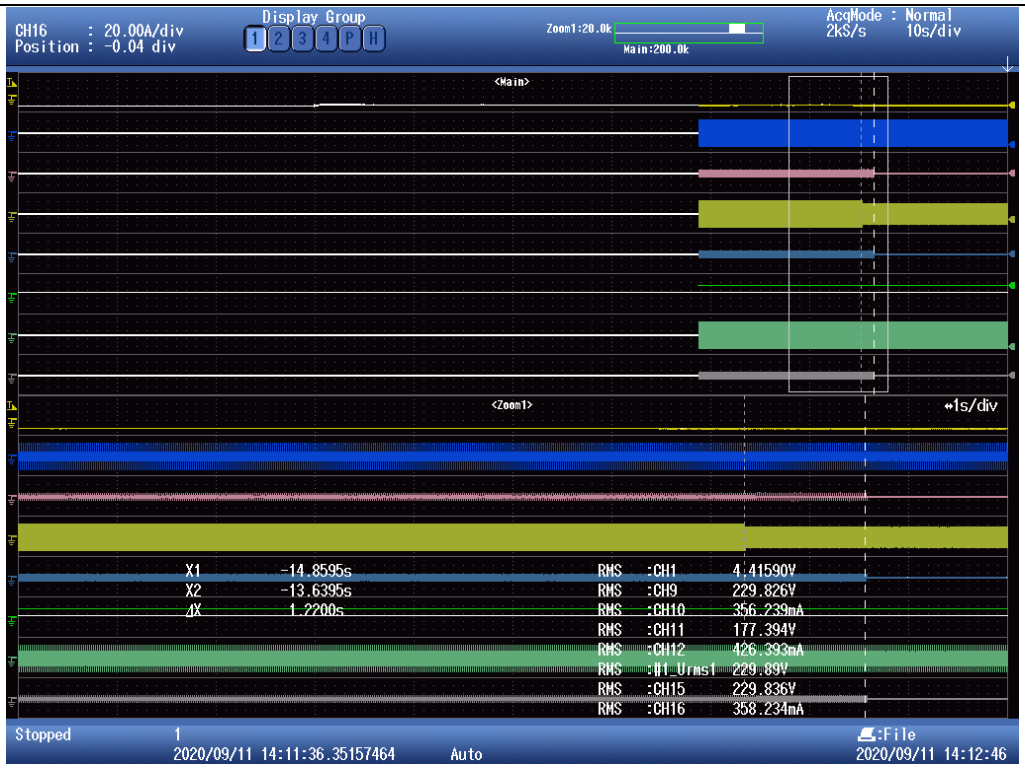
Test 2: Phases L1 disconnection time



Test 3: Phases L1 disconnection time

Test 1: Phases L2 disconnection time

CH1: trip signal; CH9, CH11, CH15: Grid Voltage; CH10, CH12, CH16: Current of EUT



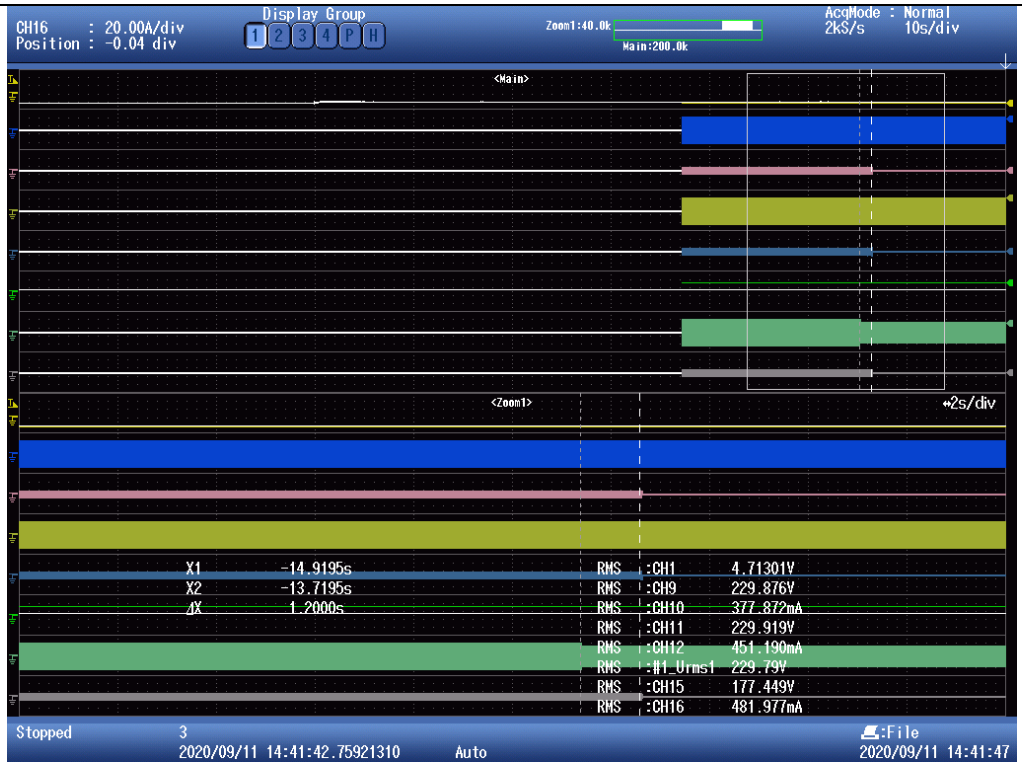
Test 2: Phases L2 disconnection time

Test 3: Phases L2 disconnection time

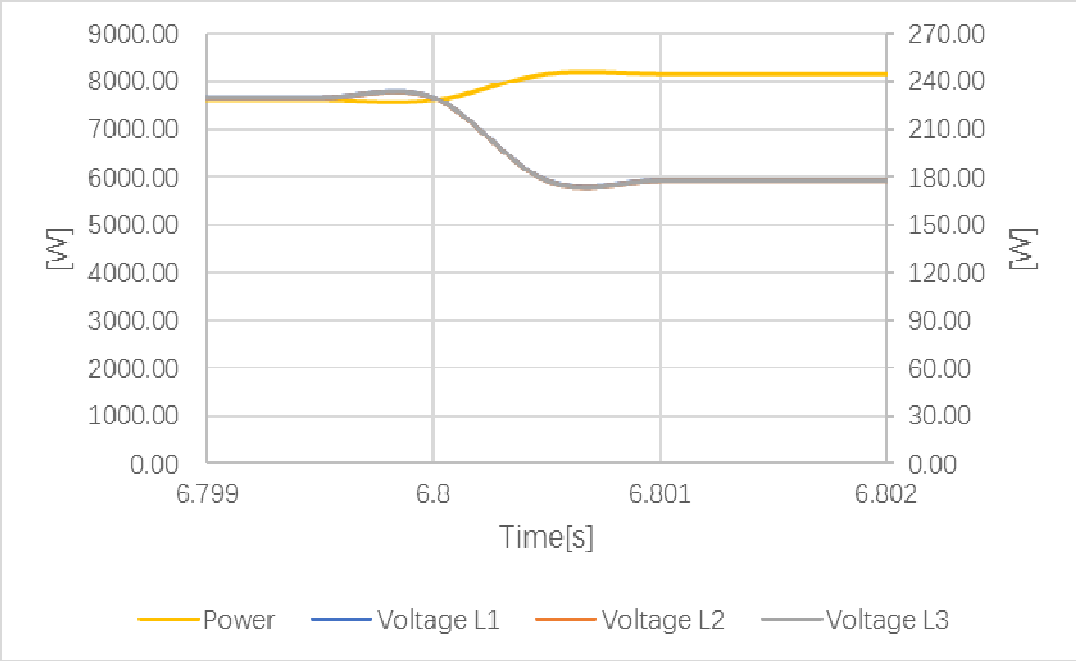
Test 1: Phases L3 disconnection time

Test 2: Phases L3 disconnection time

CH1: trip signal; CH9, CH11, CH15: Grid Voltage; CH10, CH12, CH16: Current of EUT



Test 3: Phases L3 disconnection time



Voltage drop time

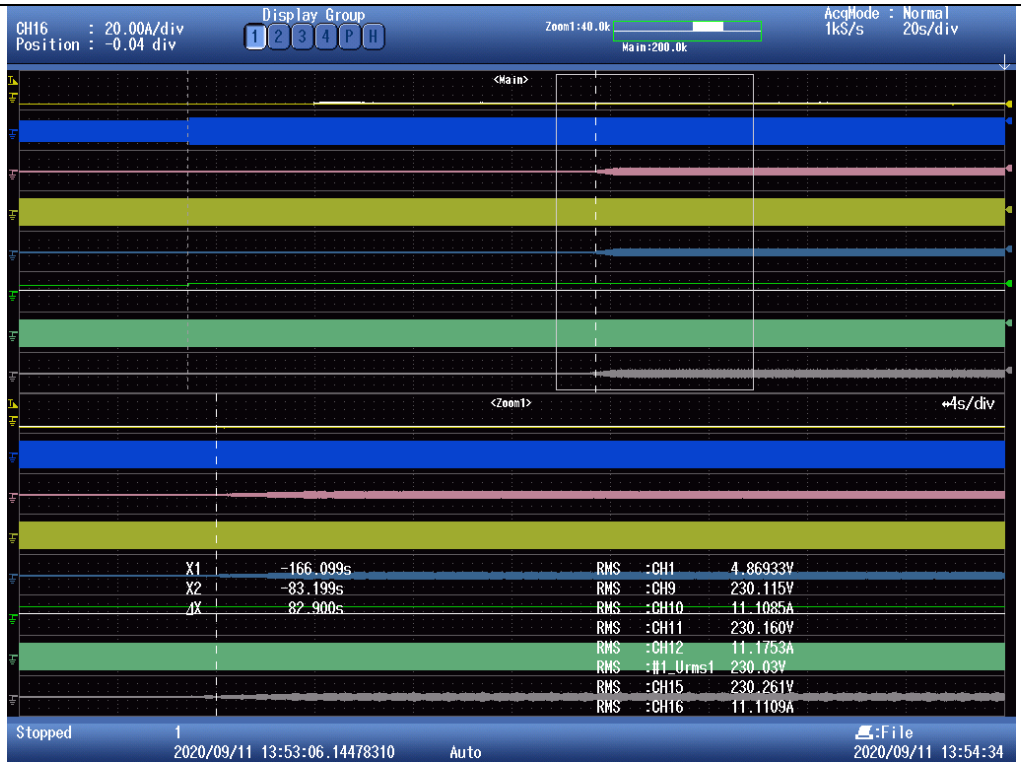
Test 1: All phases reconnection time

Test 2: All phases reconnection time

CH1: trip signal; CH9, CH11, CH15: Grid Voltage; CH10, CH12, CH16: Current of EUT

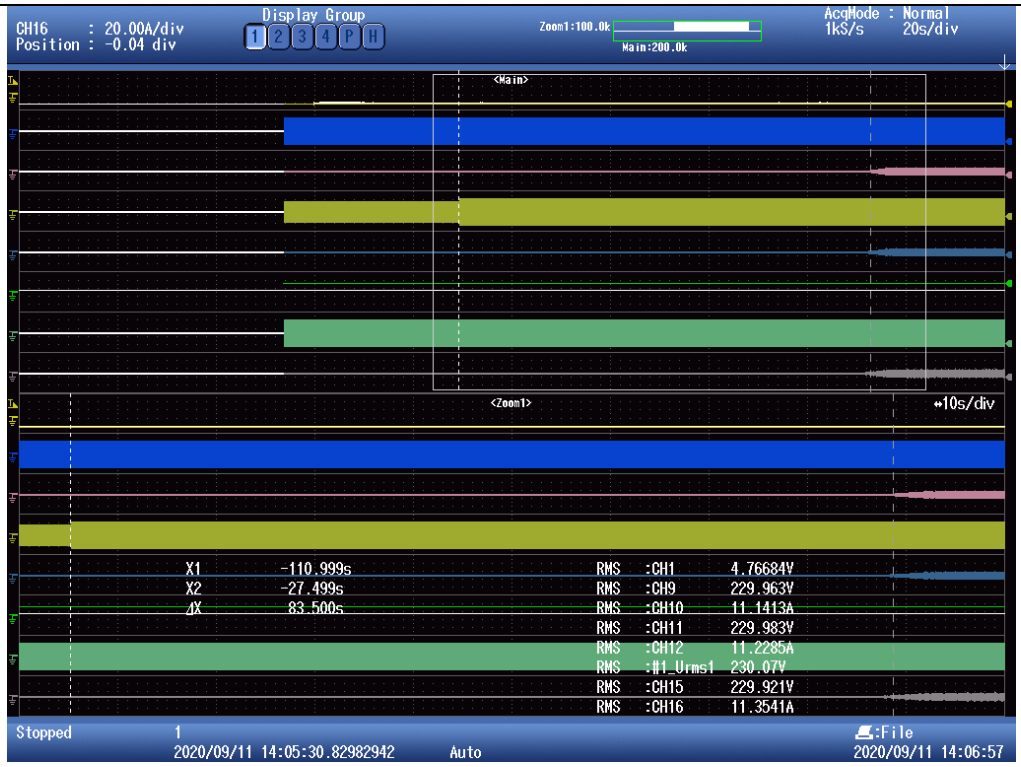
Test 3: All phases reconnection time

Test 1: Phase L1 reconnection time

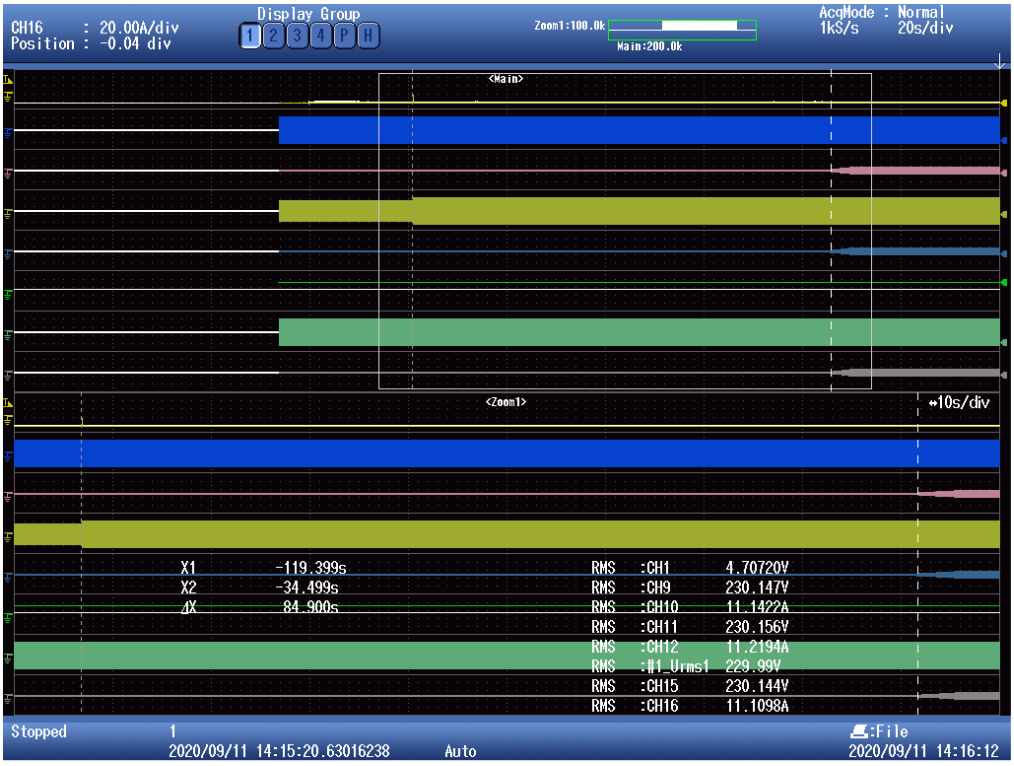


Test 2: Phase L1 reconnection time

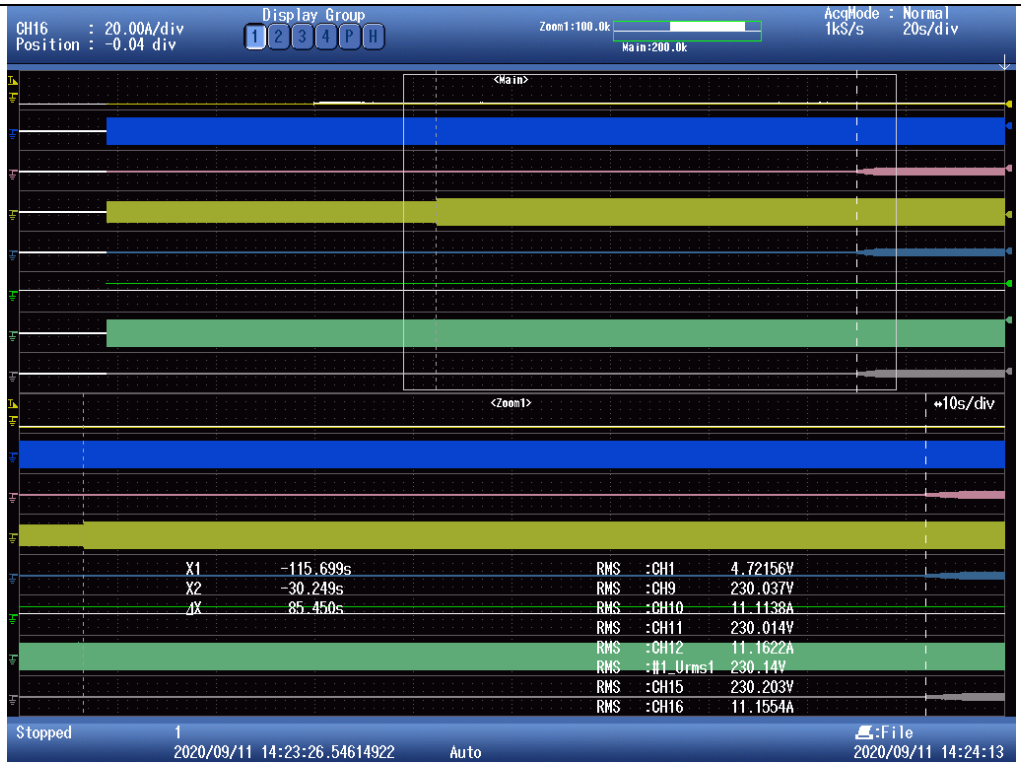
Test 3: Phase L1 reconnection time



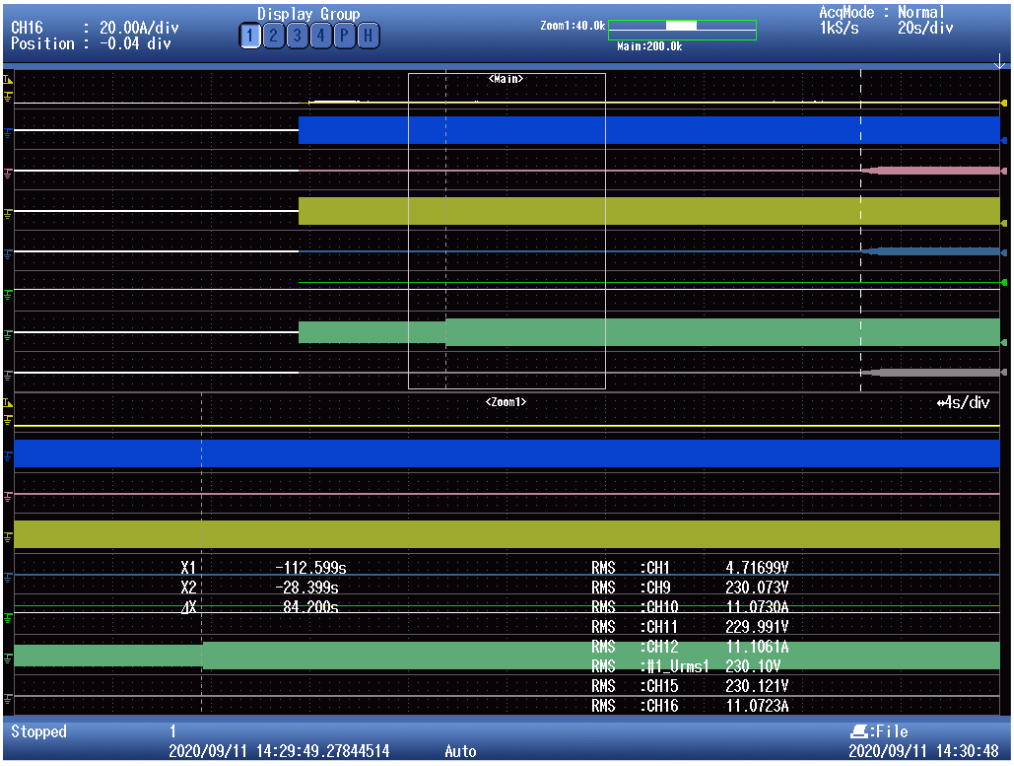
Test 1: Phase L2 reconnection time



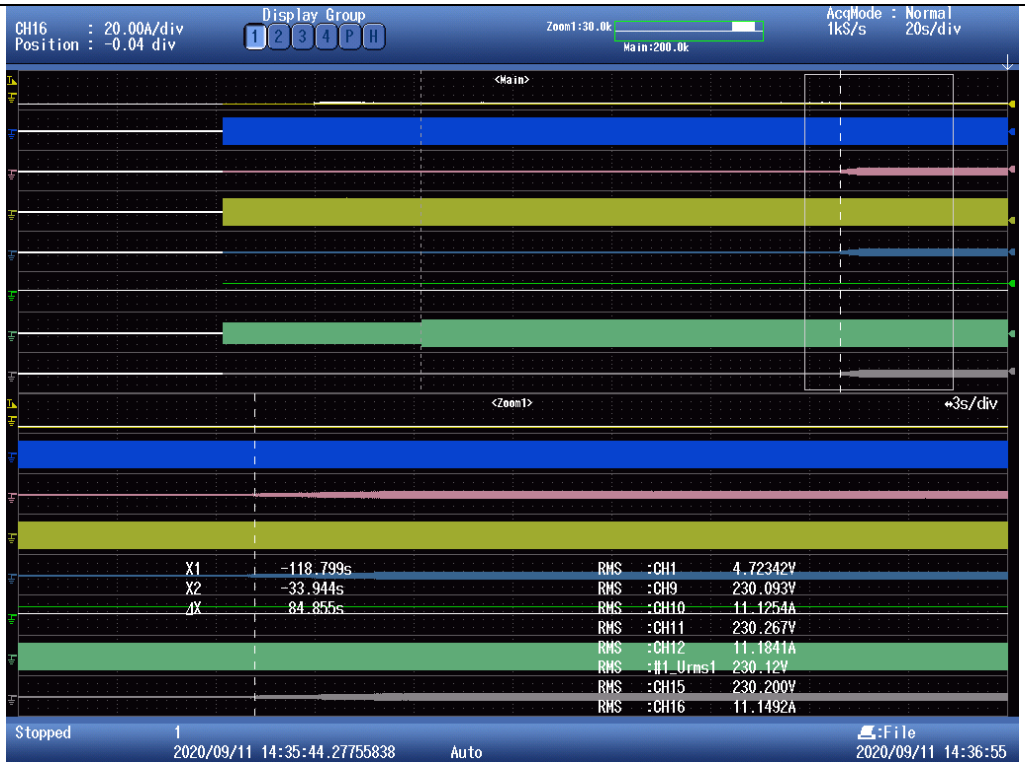
Test 2: Phase L2 reconnection time



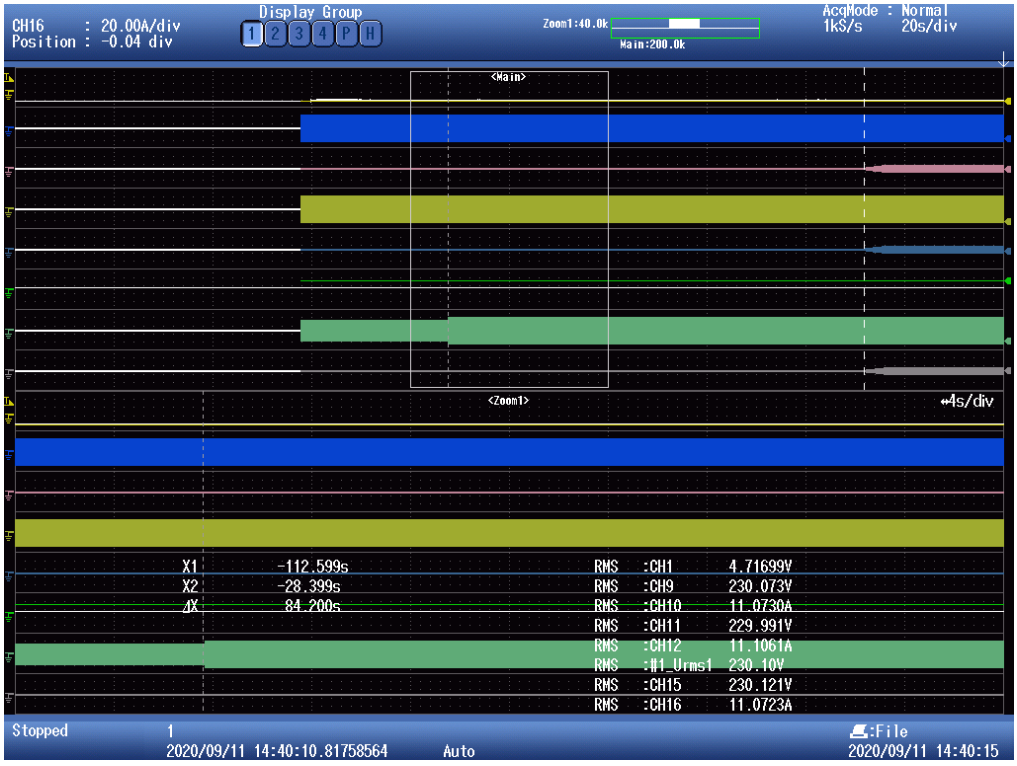
Test 3: Phase L2 reconnection time



Test 1: Phase L3 reconnection time



Test 2: Phase L3 reconnection time



Test 3: Phase L3 reconnection time

3.2 Undervoltage (V<) withstand test in response to event duration of less than trip delay time

Grid source voltage	230V	Test at 50 ±5% rated output current (A):	11.12/11.17/11.13

All phases

Test step	Grid source voltage Setting (V)	Grid source voltage measured (V)			Remain time duration (220ms) Time measured (ms)			Power recovery time measured (ms)		
		Test 1	Test 2	Test 3	Test 1	Test 2	Test 3	Test 1	Test 2	Test 3
a)	230	230.13/ 230.17/ 229.96	230.29/ 230.13/ 230.08	230.21/ 230.21/ 229.58	--	--	--	--	--	--
b)	50	50.17/ 50.04/ 50.00	50.13/ 50.08/ 50.04	50.04/ 50.08/ 50.13	240	240	240	--	--	--
c)	230	228.96/ 229.38/ 228.38	230.00/ 229.83/ 229.83	230.13/ 230.08/ 230.21	--	--	--	160.0	160.0	160.0

Phase L1

Test step	Grid source voltage Setting (V)	Grid source voltage measured (V)			Remain time duration (220ms) Time measured (ms)			Power recovery time measured (ms)		
		Test 1	Test 2	Test 3	Test 1	Test 2	Test 3	Test 1	Test 2	Test 3
a)	230	230.17	229.33	229.00	--	--	--	--	--	--
b)	50	50.04	50.13	50.04	240	240	240	--	--	--
c)	230	229.63	229.71	229.67	--	--	--	180.0	240.0	200.0

Phase L2

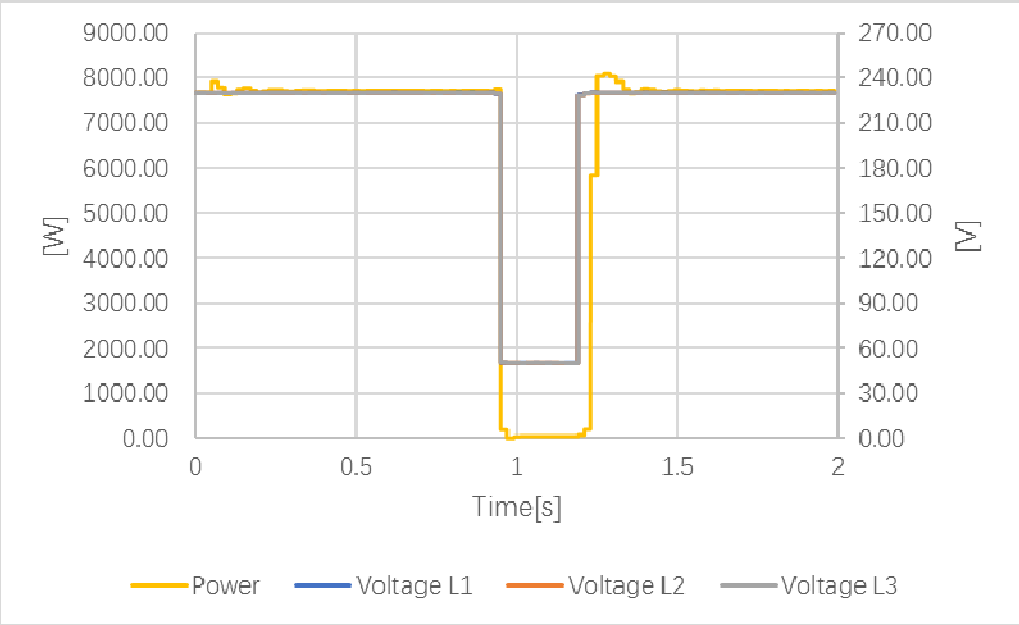
Test step	Grid source voltage Setting (V)	Grid source voltage measured (V)			Remain time duration (220ms) Time measured (ms)			Power recovery time measured (ms)		
		Test 1	Test 2	Test 3	Test 1	Test 2	Test 3	Test 1	Test 2	Test 3
a)	230	229.92	230.13	229.83	--	--	--	--	--	--
b)	50	50.00	50.00	50.04	240	240	240	--	--	--
c)	230	229.75	228.88	230.13	--	--	--	180.0	200.0	200.0

Phase L3										
Test step	Grid source voltage Setting (V)	Grid source voltage measured (V)			Remain time duration (220ms) Time measured (ms)			Power recovery time measured (ms)		
		Test 1	Test 2	Test 3	Test 1	Test 2	Test 3	Test 1	Test 2	Test 3
a)	230	229.83	229.92	230.08	--	--	--	--	--	--
b)	50	50.00	49.96	50.00	240	240	240	--	--	--
c)	230	229.75	229.54	229.83	--	--	--	160.0	160.0	160.0

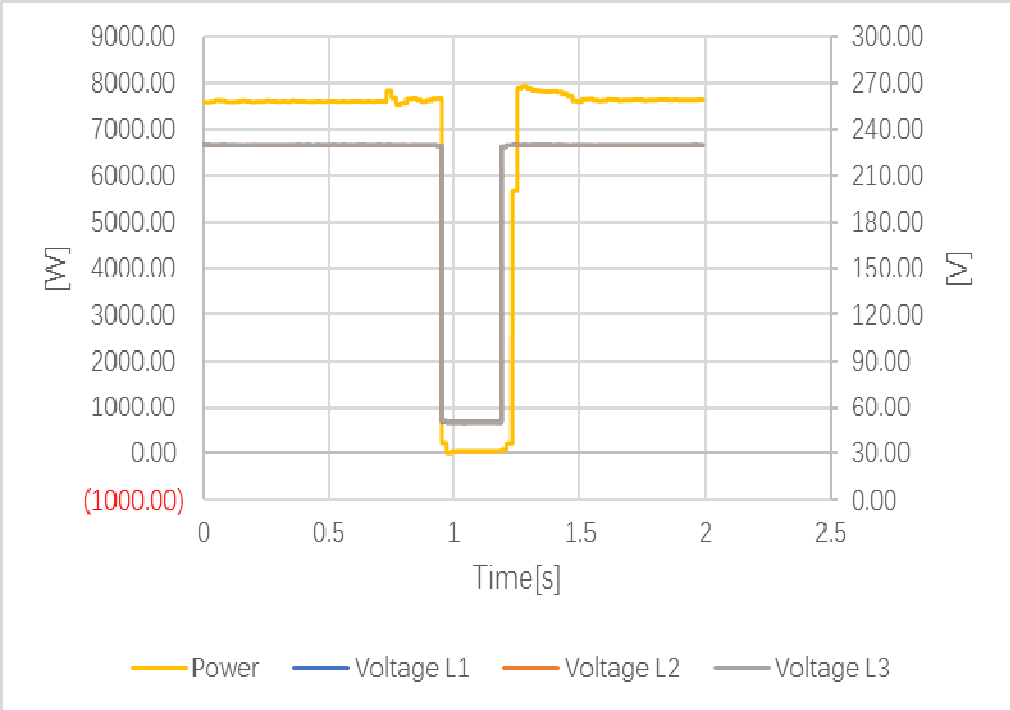
Test step	Voltage drop time measured	Voltage drop time Limited
a)→b)	1.0ms	2ms
b)→c)	1.0ms	2ms

Test Number	Power measured	
	Before voltage drop	Power recovery
All phases		
Test 1	7670.80W	7725.00W
Test 2	7595.80W	7643.80W
Test 3	7612.50W	7641.70W
Phase L1		
Test 1	7620.80W	7610.40W
Test 2	7595.80W	7637.50W
Test 3	7614.60W	7716.70W
Phase L2		
Test 1	7608.30W	7716.60W
Test 2	7610.40W	7720.80W
Test 3	7706.30W	7714.60W
Phase L3		
Test 1	7618.80W	7716.70W
Test 2	7645.80W	7658.30W
Test 3	7652.10W	7716.70W

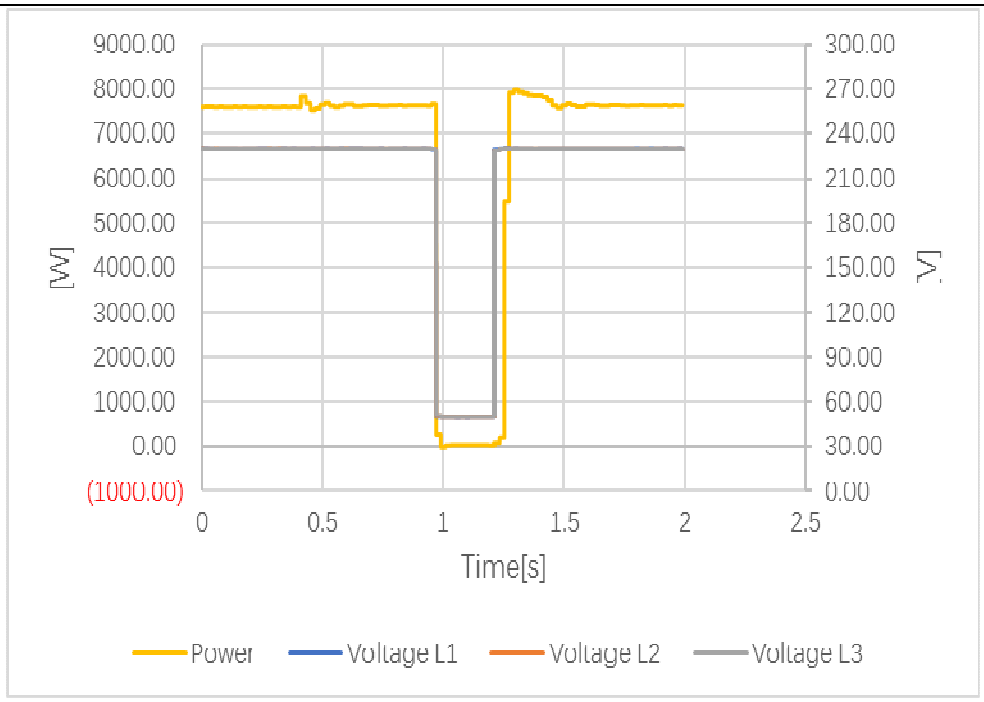
Undervoltage (V<) withstand test in response to event duration of less than trip delay time



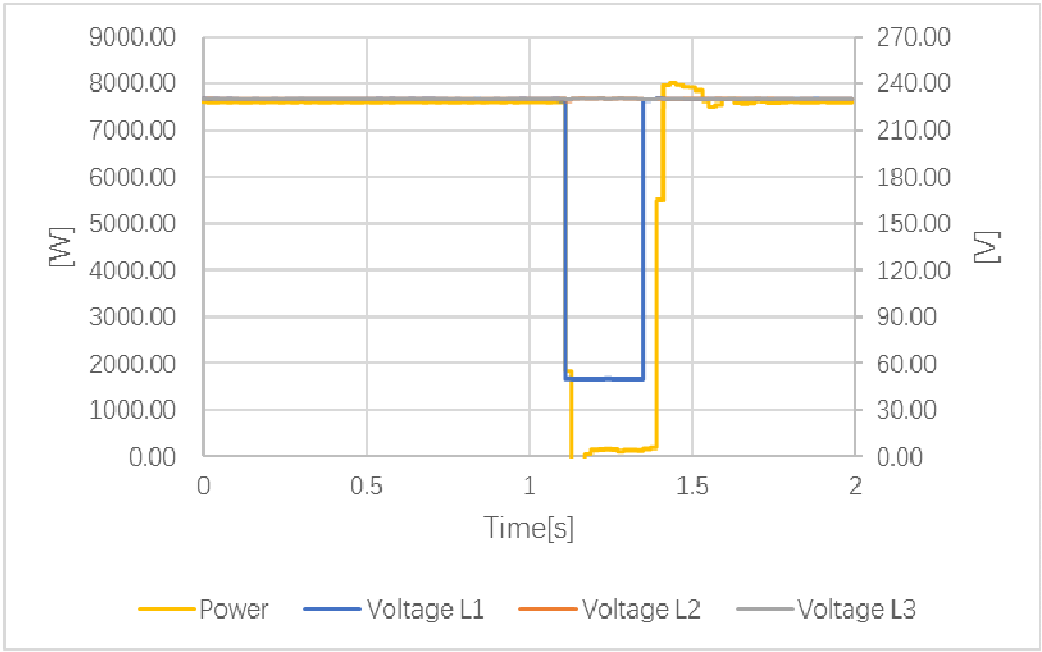
Test 1: All phases undervoltage process



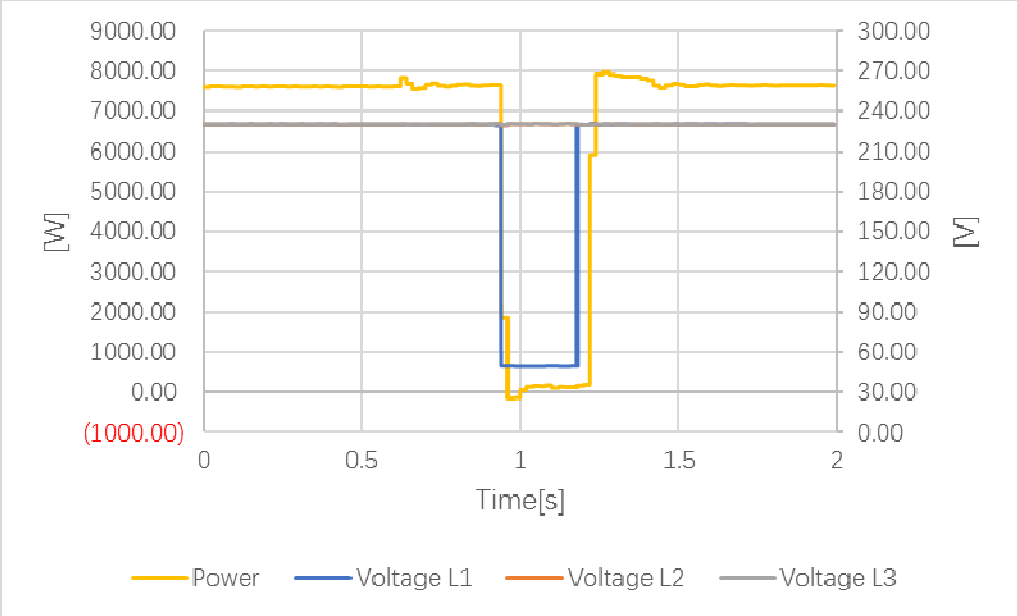
Test 2: All phases undervoltage process



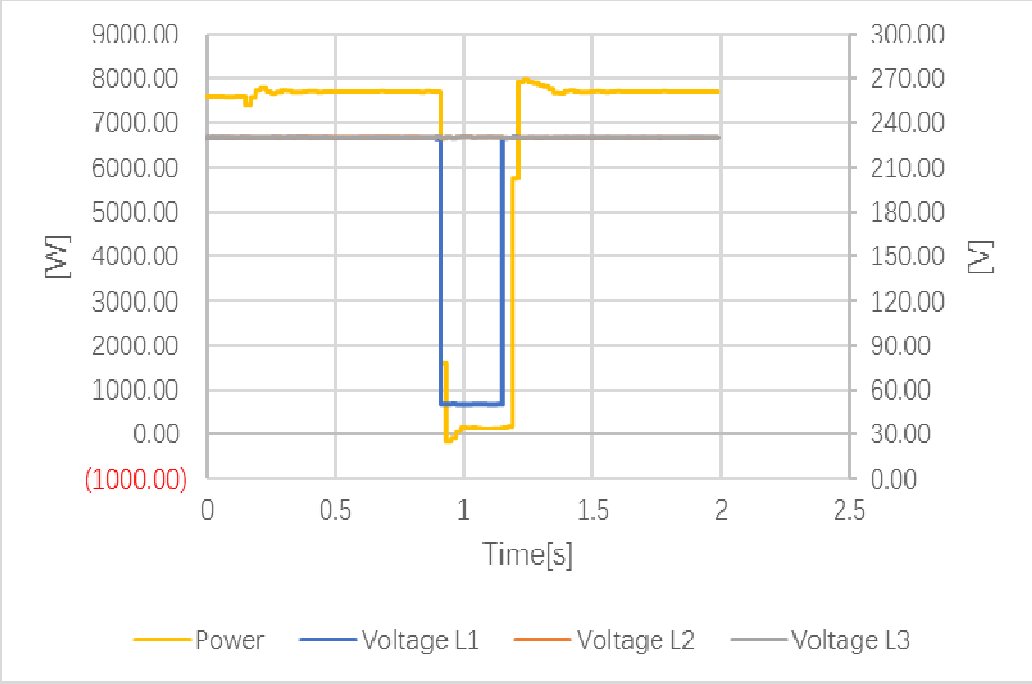
Test 3: All phases undervoltage process



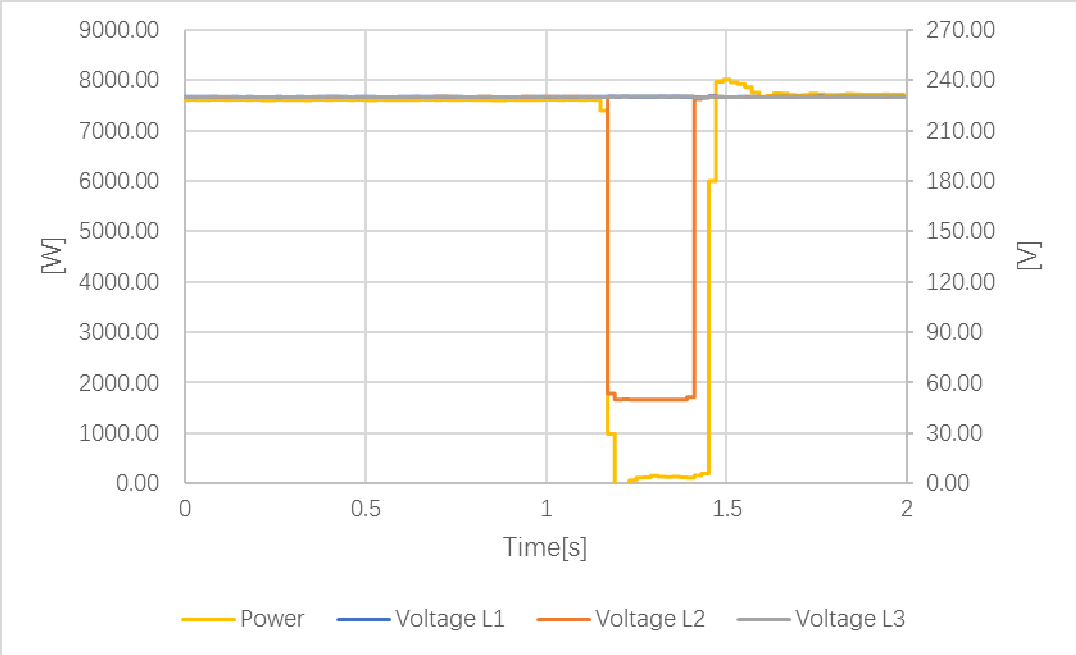
Test 1: Phase L1 undervoltage process



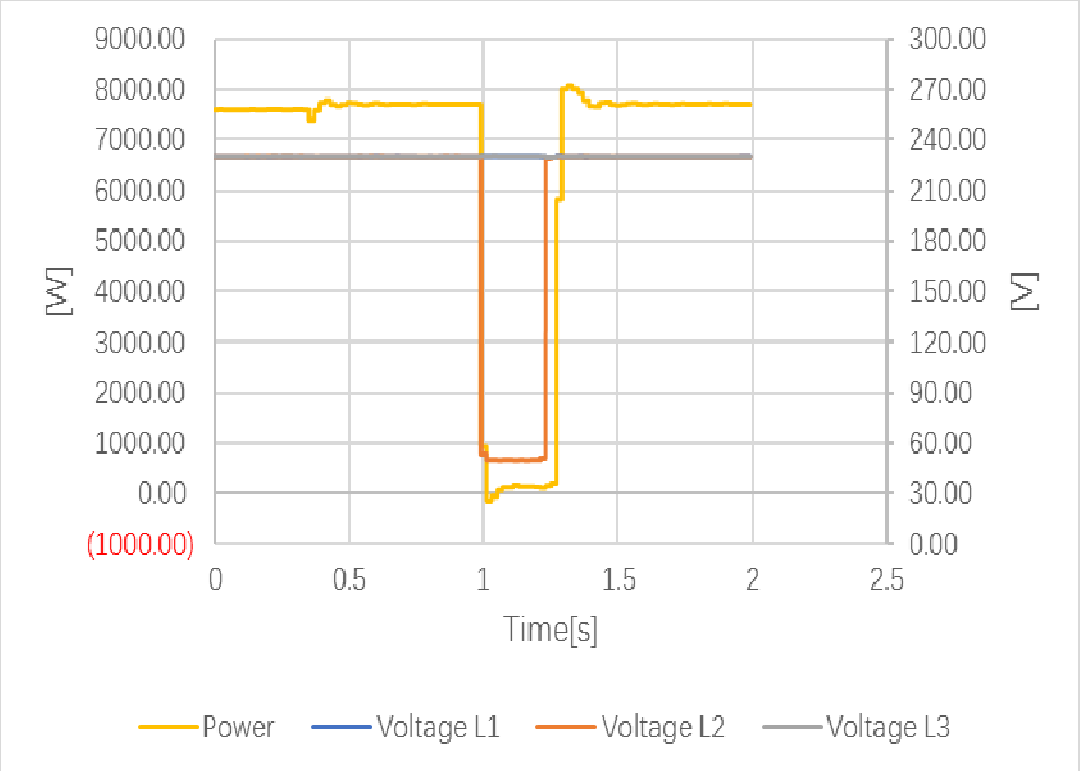
Test 2: Phase L1 undervoltage process



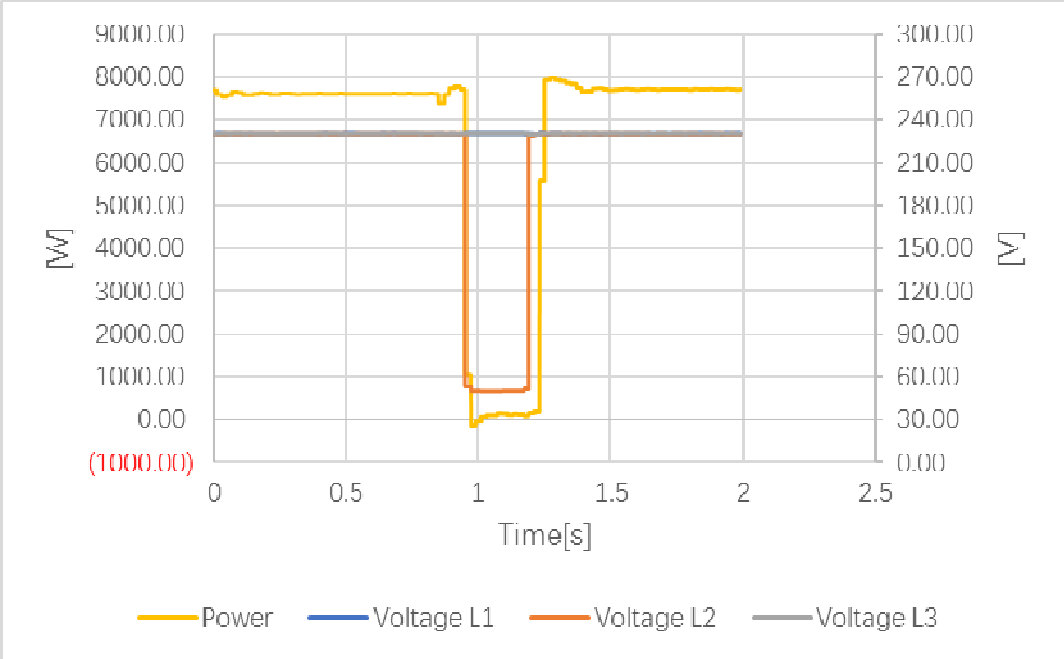
Test 3: Phase L1 undervoltage process



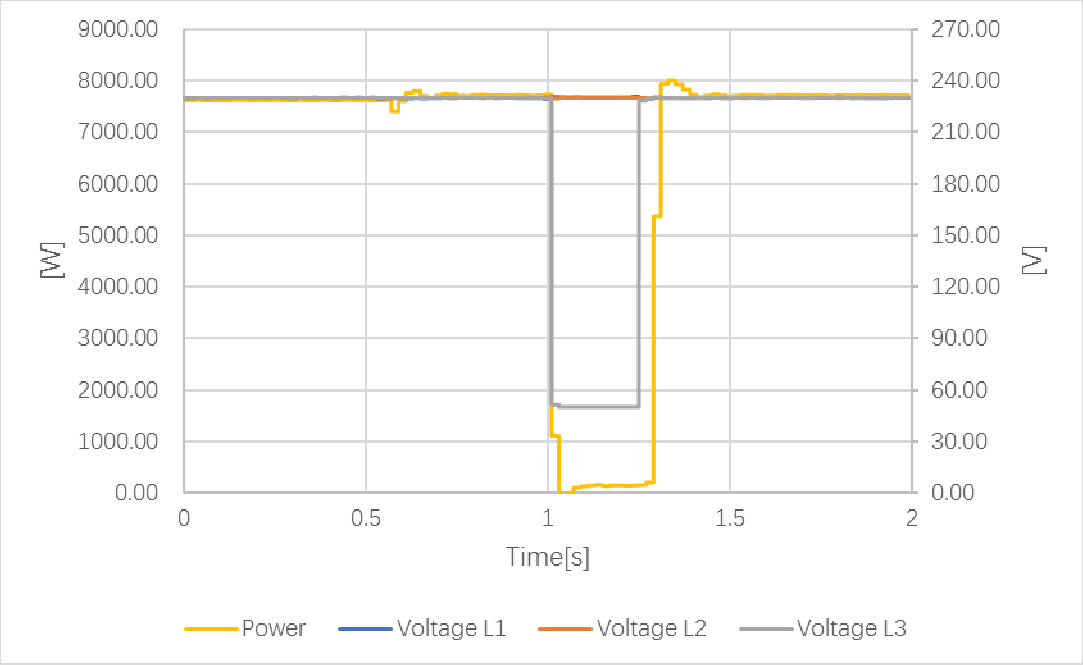
Test 1: Phase L2 undervoltage process



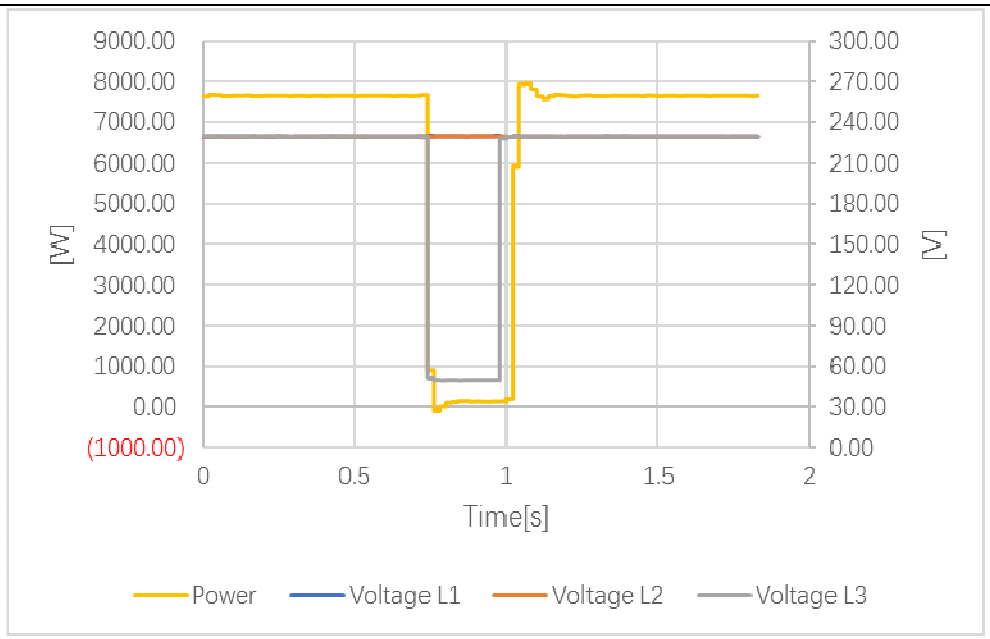
Test 2: Phase L2 undervoltage process



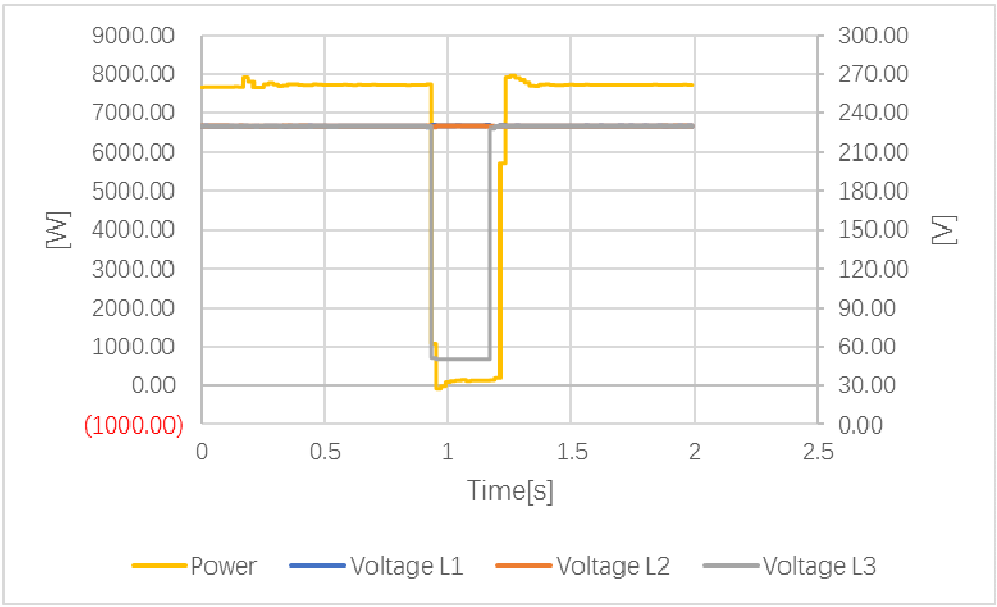
Test 3: Phase L2 undervoltage process



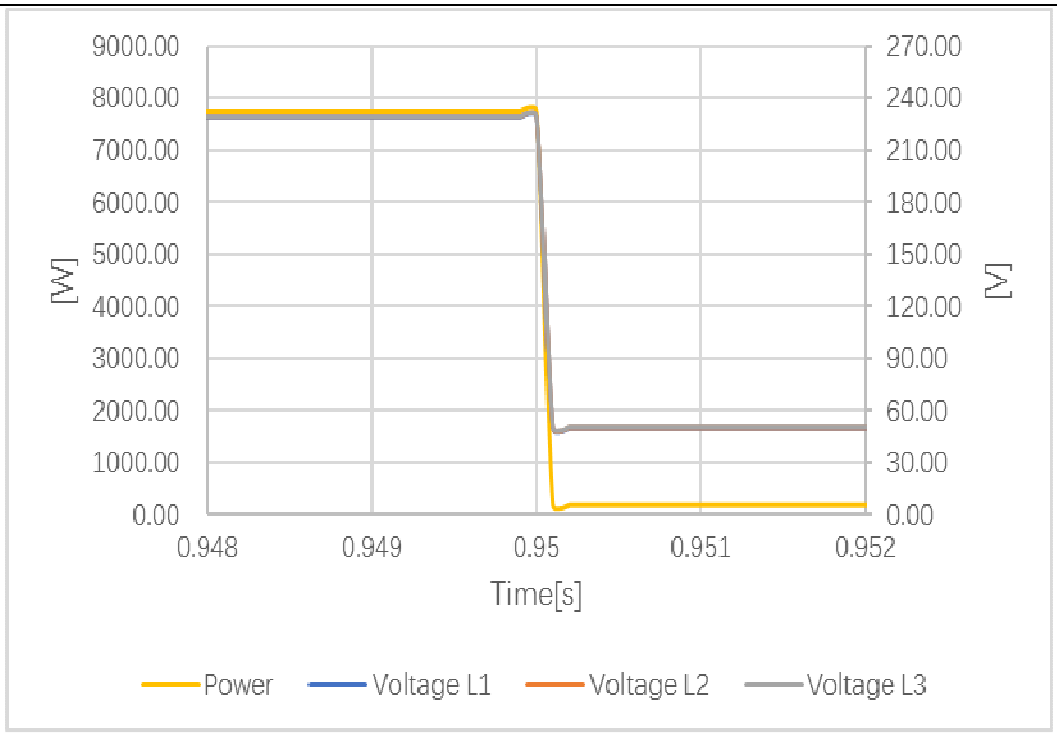
Test 1: Phase L3 undervoltage process



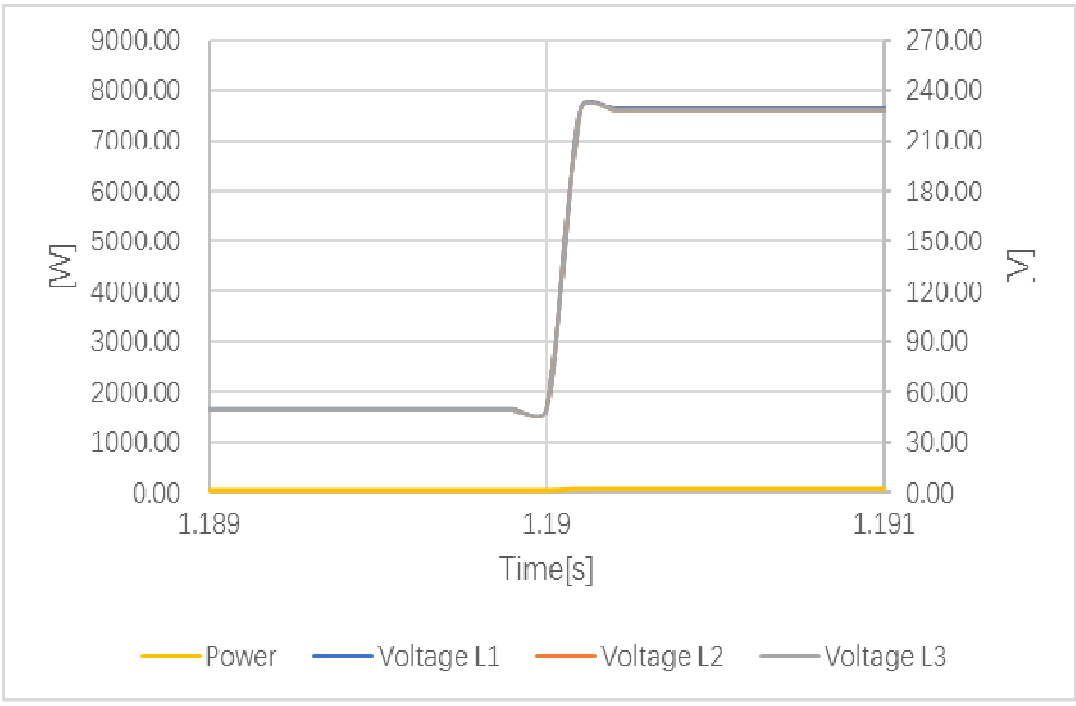
Test 2: Phase L3 undervoltage process



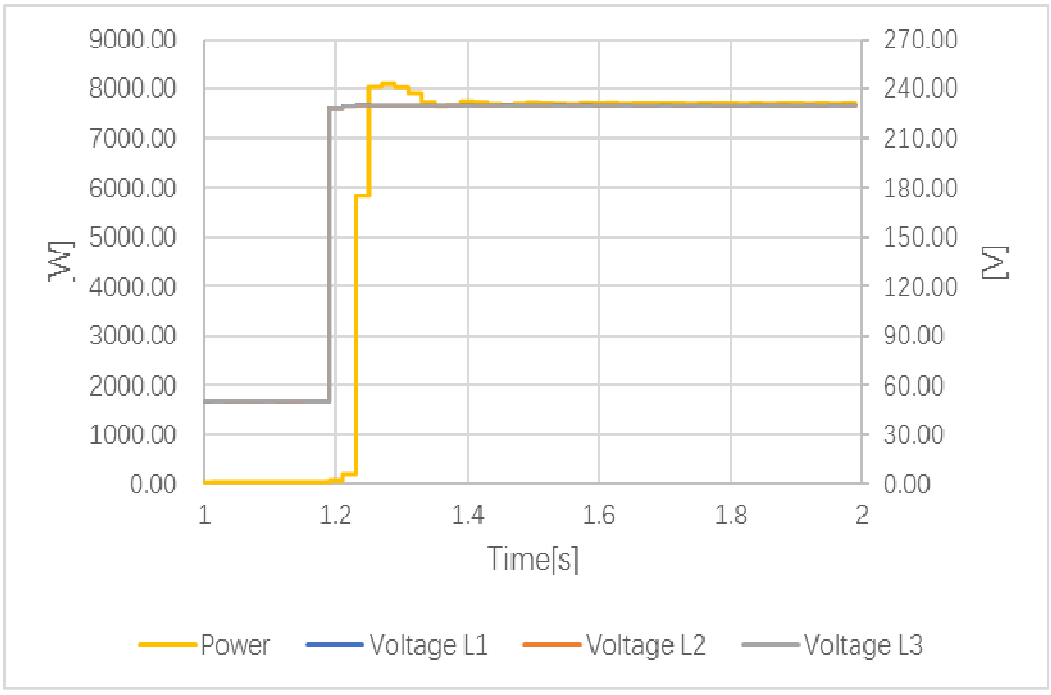
Test 3: Phase L3 undervoltage process



Voltage drop



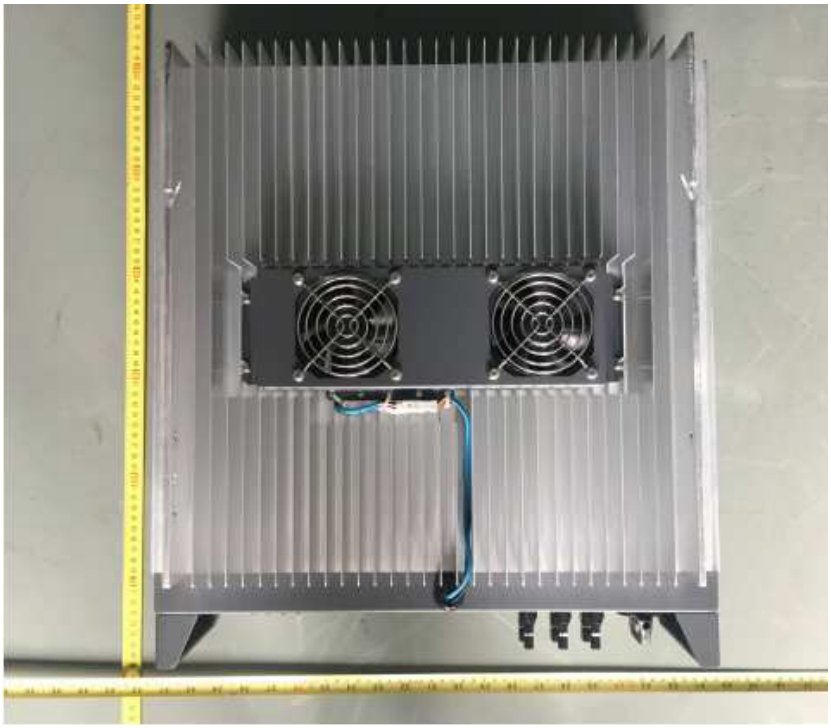
Voltage recovery



Power recovery

Photos

Front view of inverter



Rear view

(End of Report)